# HM514410B/BL Series

**1,048,576-word × 4-bit Dynamic RAM**

The Hitachi HM514410B/BL is a CMOS dynamic RAM organized 1,048,576-word × 4-bit. HM514410B/BL has realized higher density, higher performance and various functions by employing 0.8 µm CMOS process technology and some new CMOS circuit design technologies. The HM514410B/BL offers fast page mode as a high speed access mode.

Multiplexed address input permits the HM514410B/BL to be packaged in standard 20-pin plastic SOJ and 20-pin plastic ZIP.

## Features

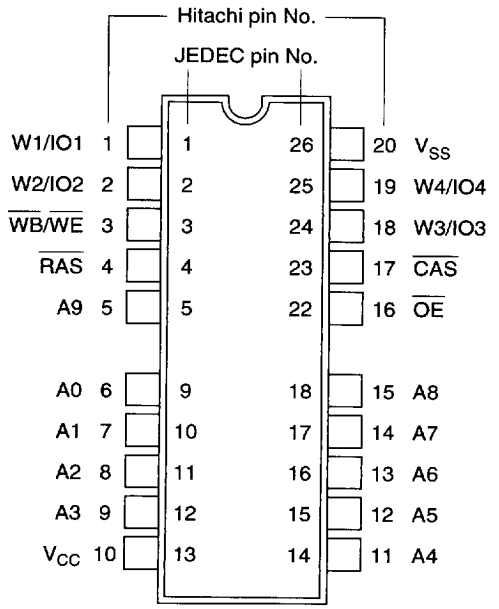
- Single 5 V (±10%)
- High speed
  - Access time: 70 ns/80 ns (max)
- Low power dissipation
  - Active mode: 550 mW/495 mW (max)
  - Standby mode: 11 mW (max)
    0.55 mW (L-version)
- Fast page mode capabillity
- 1,024 refresh cycles: 16 ms
  1,024 refresh cycles: 128 ms (L-version)
- 3 variations of refresh
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - Hidden refresh
- Test function
- Write per bit capability
- Battery back up operation
  (L-version)

## Ordering Information

| Type No. | Access time | Package |
|---|---|---|
| HM514410BS/BLS-7 | 70 ns | 300-mil 20-pin plastic SOJ (CP-20D) |
| HM514410BS/BLS-8 | 80 ns | |
| HM514410BZ/BLZ-7 | 70 ns | 400-mil 20-pin plastic ZIP (ZP-20) |
| HM514410BZ/BLZ-8 | 80 ns | |

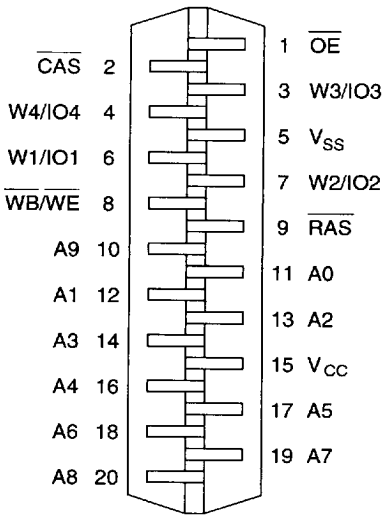
## Pin Arrangement

HM514410BS/BLS Series




(Top View)

HM514410BZ/BLZ Series

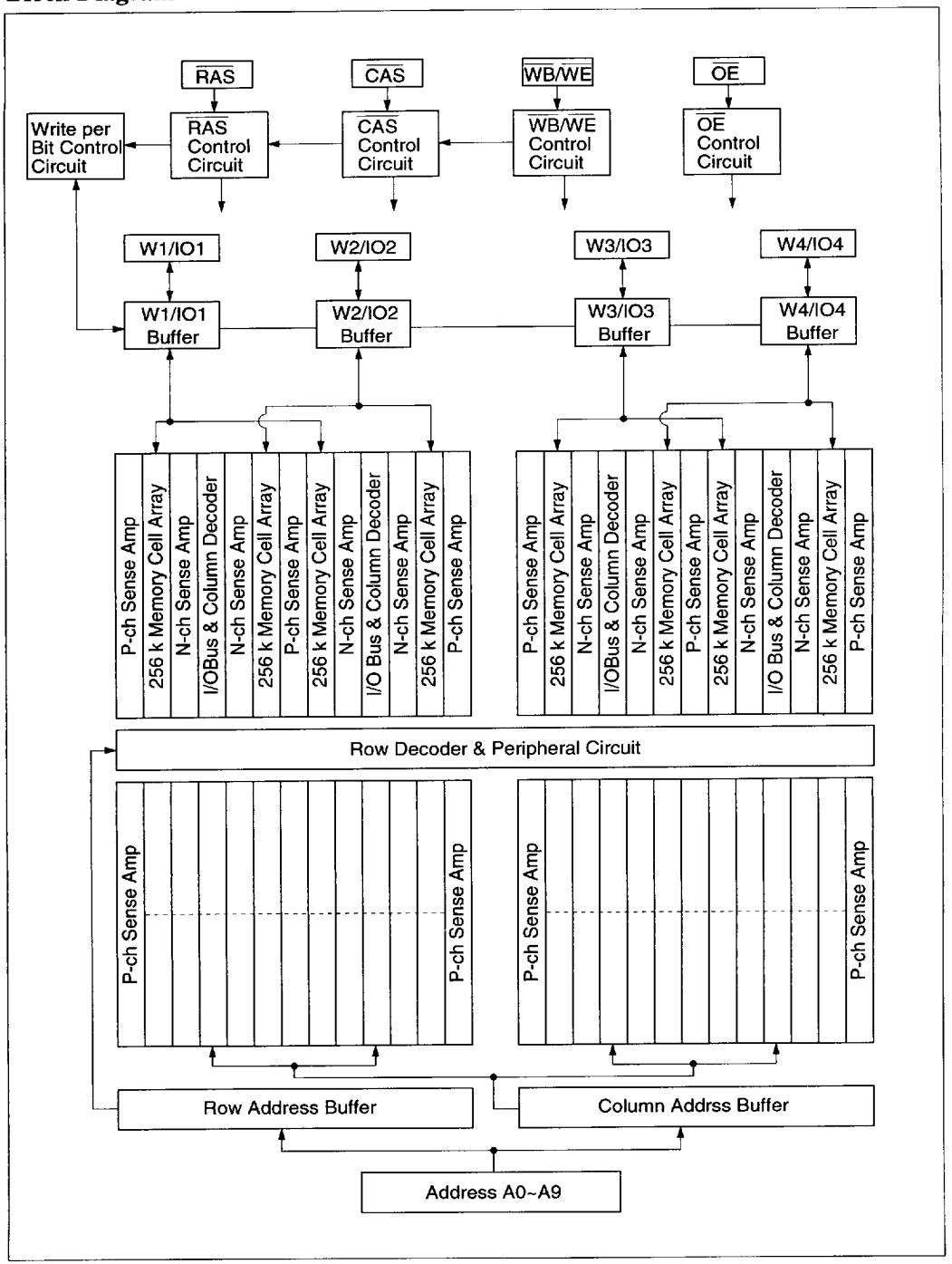



(Bottom View)

## Pin Description

| Pin Name | Function |
|---|---|
| A0 – A9 | Address input |
| A0 – A9 | Refresh address input |
| W1/IO1 – W4/IO4 | Write select/data-in/data-out |
| $\overline{RAS}$ | Row address strobe |
| $\overline{CAS}$ | Column address strobe |
| $\overline{WB/WE}$ | Write per bit/write enable |
| $\overline{OE}$ | Output enable |
| $V_{CC}$ | Power (+5 V) |
| $V_{SS}$ | Ground |

## Block Diagram



## Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Voltage on any pin relative to $V_{SS}$ | $V_T$ | −1.0 to +7.0 | V |
| Supply voltage relative to $V_{SS}$ | $V_{CC}$ | −1.0 to +7.0 | V |
| Short circuit output current | Iout | 50 | mA |
| Power dissipation | $P_T$ | 1.0 | W |
| Operating temperature | Topr | 0 to +70 | °C |
| Storage temperature | Tstg | −55 to +125 | °C |

## Recommended DC Operating Conditions (Ta = 0 to +70°C)

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{SS}$ | 0 | 0 | 0 | V | |
| | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | 1 |
| Input high voltage | $V_{IH}$ | 2.4 | — | 6.5 | V | 1 |
| Input low voltage | $V_{IL}$ | −1.0 | — | 0.8 | V | 1 |

Note: 1. All voltage referenced to $V_{SS}$

## DC Characteristics (Ta = 0 to +70°C, $V_{CC}$ = 5 V ± 10%, $V_{SS}$ = 0 V)

| | | HM514410 B/BL-7 | | HM514410 B/BL-8 | | | | |
|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | Min | Max | Min | Max | Unit | Test conditions | Notes |
| Operating current | $I_{CC1}$ | — | 100 | — | 90 | mA | $\overline{RAS}$, $\overline{CAS}$ cycling<br>$t_{RC}$ = min | 1, 2 |
| Standby current | $I_{CC2}$ | — | 2 | — | 2 | mA | TTL interface<br>$\overline{RAS}$, $\overline{CAS}$ = $V_{IH}$<br>Dout = High-Z | |
| | | — | 1 | — | 1 | mA | CMOS interface<br>$\overline{RAS}$, $\overline{CAS}$ ≥<br>$V_{CC}$ − 0.2 V<br>Dout = High-Z | |

## DC Characteristics (Ta = 0 to +70°C, $V_{CC}$ = 5 V ± 10%, $V_{SS}$ = 0 V) (cont)

| Parameter | Symbol | HM514410 B/BL-7 Min | HM514410 B/BL-7 Max | HM514410 B/BL-8 Min | HM514410 B/BL-8 Max | Unit | Test conditions | Notes |
|---|---|---|---|---|---|---|---|---|
| Standby current (L-version) | $I_{CC2}$ | — | 100 | — | 100 | µA | CMOS interface<br>$\overline{RAS}$, $\overline{CAS}$ = $V_{IH}$<br>$\overline{WE}$, $\overline{OE}$, address,<br>Din = $V_{IH}$ or $V_{IL}$<br>Dout = High-Z | 4 |
| $\overline{RAS}$-only refresh current | $I_{CC3}$ | — | 100 | — | 90 | mA | $t_{RC}$ = min | 2 |
| Standby current | $I_{CC5}$ | — | 5 | — | 5 | mA | $\overline{RAS}$ = $V_{IH}$<br>$\overline{CAS}$ = $V_{IL}$<br>Dout = enable | 1 |
| $\overline{CAS}$-before-$\overline{RAS}$ refresh current | $I_{CC6}$ | — | 100 | — | 90 | mA | $t_{RC}$ = min | |
| Fast page mode current | $I_{CC7}$ | — | 100 | — | 90 | mA | $t_{PC}$ = min | 1, 3 |
| Battery back up operation current (Standby with CBR refresh) (L-version) | $I_{CC10}$ | — | 200 | — | 200 | µA | $t_{RC}$ = 125 µs<br>$t_{\overline{RAS}}$ ≤ 1 µs<br>$\overline{WE}$ = $V_{IH}$,<br>$\overline{CAS}$ = $V_{IL}$,<br>$\overline{OE}$, address,<br>Din = $V_{IH}$ or $V_{IL}$<br>Dout = High-Z | 4 |
| Input leakage current | $I_{LI}$ | –10 | 10 | –10 | 10 | µA | 0 V ≤ Vin ≤ 7 V | |
| Output leakage current | $I_{LO}$ | –10 | 10 | –10 | 10 | µA | 0 V ≤ Vout ≤ 7 V<br>Dout = disable | |
| Output high voltage | $V_{OH}$ | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | V | High Iout = –5 mA | |
| Output low voltage | $V_{OL}$ | 0 | 0.4 | 0 | 0.4 | V | Low Iout = 4.2 mA | |

Notes: 1. $I_{CC}$ depends on output load condition when the device is selected. $I_{CC}$ max is specified at the output open condition.
2. Address can be changed twice or less while $\overline{RAS}$ = $V_{IL}$.
3. Address can be changed once or less while $\overline{CAS}$ = $V_{IH}$.
4. $V_{CC}$ – 0.2 V ≤ $V_{IH}$ ≤ 6.5 V, 0 V ≤ $V_{IL}$ ≤ 0.2 V

## Capacitance (Ta = 25°C, $V_{CC}$ = 5 V ± 10%)

| Parameter | Symbol | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input capacitance (Address) | $C_{I1}$ | — | 5 | pF | 1 |
| Input capacitance (Clocks) | $C_{I2}$ | — | 7 | pF | 1 |
| Output capacitance (Data-in, data-out) | $C_{I/O}$ | — | 7 | pF | 1, 2 |

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = $V_{IH}$ to disable Dout.

## AC Characteristics (Ta = 0 to +70°C, $V_{CC}$ = 5 V ± 10%, $V_{SS}$ = 0 V) *1, *14, *15, *16

### Test Conditions

- Input rise and fall times: 5ns
- Input timing reference levels: 0.8 V, 2.4 V
- Output load: 2 TTL gate +$C_L$ (100 pF) (Including scope and jig)

### Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

| | | HM514410B/BL-7 | | HM514410B/BL-8 | | | |
|---|---|---|---|---|---|---|---|
| Parameter | Symbol | Min | Max | Min | Max | Unit | Notes |
| Random read or write cycle time | $t_{RC}$ | 130 | — | 150 | — | ns | |
| $\overline{RAS}$ precharge time | $t_{RP}$ | 50 | — | 60 | — | ns | |
| $\overline{RAS}$ pulse width | $t_{RAS}$ | 70 | 10000 | 80 | 10000 | ns | 21 |
| $\overline{CAS}$ pulse width | $t_{CAS}$ | 20 | 10000 | 20 | 10000 | ns | 22 |
| Row address setup time | $t_{ASR}$ | 0 | — | 0 | — | ns | |
| Row address hold time | $t_{RAH}$ | 10 | — | 10 | — | ns | |
| Column address setup time | $t_{ASC}$ | 0 | — | 0 | — | ns | |
| Column address hold time | $t_{CAH}$ | 15 | — | 15 | — | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ delay time | $t_{RCD}$ | 20 | 50 | 20 | 60 | ns | 8 |
| $\overline{RAS}$ to column address delay time | $t_{RAD}$ | 15 | 35 | 15 | 40 | ns | 9 |
| $\overline{RAS}$ hold time | $t_{RSH}$ | 20 | — | 20 | — | ns | |
| $\overline{CAS}$ hold time | $t_{CSH}$ | 70 | — | 80 | — | ns | |
| $\overline{CAS}$ to $\overline{RAS}$ precharge time | $t_{CRP}$ | 10 | — | 10 | — | ns | |
| $\overline{OE}$ to Din delay time | $t_{ODD}$ | 20 | — | 20 | — | ns | |

**Read, Write, Read-Modify-Write and Refresh Cycles** (Common Parameters) (cont)

| | | HM514410B/BL-7 | | HM514410B/BL-8 | | | |
|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** | **Notes** |
| $\overline{OE}$ delay time from Din | $t_{DZO}$ | 0 | — | 0 | — | ns | |
| $\overline{CAS}$ setup time from Din | $t_{DZC}$ | 0 | — | 0 | — | ns | |
| Transition time (rise and fall) | $t_T$ | 3 | 50 | 3 | 50 | ns | 7 |
| Refresh period | $t_{REF}$ | — | 16 | — | 16 | ms | |
| Refresh period (L-version) | $t_{REF}$ | — | 128 | — | 128 | ms | |

**Read Cycle**

| | | HM514410B/BL-7 | | HM514410B/BL-8 | | | |
|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** | **Notes** |
| Access time from $\overline{RAS}$ | $t_{RAC}$ | — | 70 | — | 80 | ns | 2, 3, 17 |
| Access time from $\overline{CAS}$ | $t_{CAC}$ | — | 20 | — | 20 | ns | 3, 4, 13, 17 |
| Access time from Address | $t_{AA}$ | — | 35 | — | 40 | ns | 3, 5, 13, 17 |
| Access time from $\overline{OE}$ | $t_{OAC}$ | — | 20 | — | 20 | ns | 3, 17 |
| Read command setup time | $t_{RCS}$ | 0 | — | 0 | — | ns | |
| Read command hold time to $\overline{CAS}$ | $t_{RCH}$ | 0 | — | 0 | — | ns | 20 |
| Read command hold time to $\overline{RAS}$ | $t_{RRH}$ | 0 | — | 0 | — | ns | 20 |
| Column address to $\overline{RAS}$ lead time | $t_{RAL}$ | 35 | — | 40 | — | ns | |
| Output buffer turn-off time | $t_{OFF1}$ | 0 | 20 | 0 | 20 | ns | 6 |
| Output buffer turn-off to $\overline{OE}$ | $t_{OFF2}$ | 0 | 20 | 0 | 20 | ns | 6 |
| $\overline{CAS}$ to Din delay time | $t_{CDD}$ | 20 | — | 20 | — | ns | |
| $\overline{OE}$ pulse width | $t_{OEP}$ | 20 | — | 20 | — | ns | |

### Write Cycle

| Parameter | Symbol | HM514410B/BL-7 Min | HM514410B/BL-7 Max | HM514410B/BL-8 Min | HM514410B/BL-8 Max | Unit | Notes |
|---|---|---|---|---|---|---|---|
| Write command setup time | $t_{WCS}$ | — | 0 | — | 0 | ns | 10 |
| Write command hold time | $t_{WCH}$ | 15 | — | 15 | — | ns | |
| Write command pulse width | $t_{WP}$ | 10 | — | 10 | — | ns | |
| Write command to $\overline{RAS}$ lead time | $t_{RWL}$ | 20 | — | 20 | — | ns | |
| Write command to $\overline{CAS}$ lead time | $t_{CWL}$ | 20 | — | 20 | — | ns | |
| Data-in setup time | $t_{DS}$ | 0 | — | 0 | — | ns | 11 |
| Data-in hold time | $t_{DH}$ | 15 | — | 15 | — | ns | 11 |

### Read-Modify-Write Cycle

| Parameter | Symbol | HM514410B/BL-7 Min | HM514410B/BL-7 Max | HM514410B/BL-8 Min | HM514410B/BL-8 Max | Unit | Notes |
|---|---|---|---|---|---|---|---|
| Read-modify-write cycle time | $t_{RWC}$ | 180 | — | 200 | — | ns | |
| $\overline{RAS}$ to $\overline{WE}$ delay time | $t_{RWD}$ | 95 | — | 105 | — | ns | 10 |
| $\overline{CAS}$ to $\overline{WE}$ delay time | $t_{CWD}$ | 45 | — | 45 | — | ns | 10 |
| Column address to $\overline{WE}$ delay time | $t_{AWD}$ | 60 | — | 65 | — | ns | 10 |
| $\overline{OE}$ hold time from $\overline{WE}$ | $t_{OEH}$ | 20 | — | 20 | — | ns | |

### Refresh Cycle

| Parameter | Symbol | HM514410B/BL-7 Min | HM514410B/BL-7 Max | HM514410B/BL-8 Min | HM514410B/BL-8 Max | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle) | $t_{CSR}$ | 10 | — | 10 | — | ns | |
| $\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle) | $t_{CHR}$ | 10 | — | 10 | — | ns | |
| $\overline{RAS}$ precharge to $\overline{CAS}$ hold time | $t_{RPC}$ | 10 | — | 10 | — | ns | |
| $\overline{CAS}$ precharge time in normal mode | $t_{CPN}$ | 10 | — | 10 | — | ns | |

### Fast Page Mode Cycle

| | | HM514410B/BL-7 | | HM514410B/BL-8 | | | |
|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** | **Notes** |
| Fast page mode cycle time | $t_{PC}$ | 45 | — | 50 | — | ns | |
| Fast page mode $\overline{CAS}$ precharge time | $t_{CP}$ | 10 | — | 10 | — | ns | |
| Fast page mode $\overline{RAS}$ pulse width | $t_{RASC}$ | — | 100000 | — | 100000 | ns | 12 |
| Access time from $\overline{CAS}$ precharge | $t_{ACP}$ | — | 40 | — | 45 | ns | 3, 13, 17 |
| $\overline{RAS}$ hold time from $\overline{CAS}$ precharge | $t_{RHCP}$ | 40 | — | 45 | — | ns | |

### Fast Page Mode Read-Modify-Write Cycle

| | | HM514410B/BL-7 | | HM514410B/BL-8 | | | |
|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** | **Notes** |
| Fast page mode read modify-write cycle time | $t_{PCM}$ | 95 | — | 100 | — | ns | |
| $\overline{CAS}$ precharge to $\overline{WE}$ delay time | $t_{CPW}$ | 65 | — | 70 | — | ns | |

### Test Mode Cycle

| | | HM514410B/BL-7 | | HM514410B/BL-8 | | | |
|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** | **Notes** |
| Test mode $\overline{WE}$ setup time | $t_{WS}$ | 0 | — | 0 | — | ns | |
| Test mode $\overline{WE}$ hold time | $t_{WH}$ | 10 | — | 10 | — | ns | |

### Counter Test Cycle

| | | HM514410B/BL-7 | | HM514410B/BL-8 | | | |
|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** | **Notes** |
| $\overline{CAS}$ precharge time in counter test cycle | $t_{CPT}$ | 40 | — | 40 | — | ns | |

**Write Per Bit** *18, *19

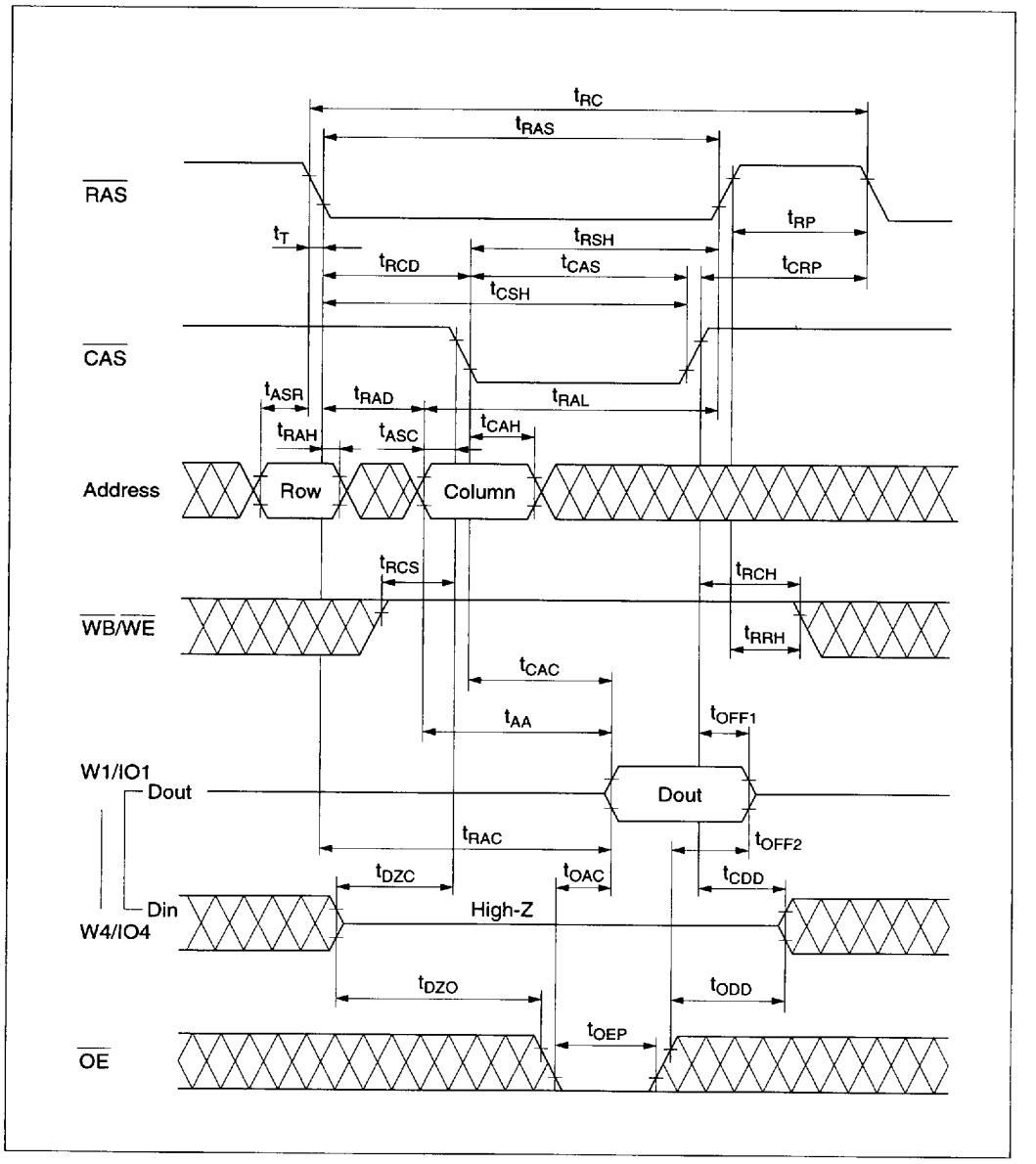
| Parameter | Symbol | HM514410B/BL-7 Min | HM514410B/BL-7 Max | HM514410B/BL-8 Min | HM514410B/BL-8 Max | Unit | Notes |
|---|---|---|---|---|---|---|---|
| Write per bit setup time | $t_{WBS}$ | 0 | — | 0 | — | ns | |
| Write per bit hold time | $t_{WBH}$ | 15 | — | 15 | — | ns | |
| Write per bit selection setup time | $t_{WDS}$ | 0 | — | 0 | — | ns | |
| Write per bit selection hold time | $t_{WDH}$ | 15 | — | 15 | — | ns | |

Notes:
1. AC measurements assume $t_T$ = 5 ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$(max). If $t_{RCD}$ or $t_{RAD}$ is greater than the maximum recommended value shown in this table, $t_{RAC}$ exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. $t_{OFF}$ (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. $V_{IH}$ (min) and $V_{IL}$ (max) are reference levels for measuring timing of input signals. Also, transition times are measured between $V_{IH}$ and $V_{IL}$.
8. Operation with the $t_{RCD}$ (max) limit insures that $t_{RAC}$ (max) can be met, $t_{RCD}$ (max) is specified as a reference point only, if $t_{RCD}$ is greater than the specified $t_{RCD}$ (max) limit, then access time is controlled exclusively by $t_{CAC}$.
9. Operation with the $t_{RAD}$ (max) limit insures that $t_{RAC}$ (max) can be met, $t_{RAD}$ (max) is specified as a reference point only, if $t_{RAD}$ is greater than the specified $t_{RAD}$ (max) limit, then access time is controlled exclusively by $t_{AA}$.
10. $t_{WCS}$, $t_{RWD}$, $t_{CWD}$, $t_{AWD}$ and $t_{CPW}$ are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min) the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. $t_{RASC}$ defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longest of $t_{AA}$ or $t_{CAC}$ or $t_{ACP}$.
14. An initial pause of 100 µs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh cycle or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before -$\overline{RAS}$ refresh cycles is required.
15. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
16. Test mode operation specified in this data sheet is 2-bit test function controlled by control address bits – CA0. This test mode operation can be performed by $\overline{WB}/\overline{WE}$-and-$\overline{CAS}$-before-$\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of two test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. In order to end this test mode operation, perform a $\overline{RAS}$-only refresh cycle or a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.
17. In a test mode read cycle, the value of $t_{RAC}$, $t_{CAC}$, $t_{AA}$, $t_{OAC}$ and $t_{ACP}$ is delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

18. When using the write-per-bit capability, $\overline{WB}/\overline{WE}$ must be low as $\overline{RAS}$ falls.
19. The data bits to which the write operation is applied can be specified by keeping W1/IO1, W2/IO2, W3/IO3 and W4/IO4 high with setup and hold time referenced to the $\overline{RAS}$ negative transition.
20. Either $t_{RCH}$ or $t_{RRH}$ shall be satisfied.
21. $t_{RAS}$ (min) = $t_{RWD}$ (min) + $t_{RWL}$ (min) + $t_T$ in read-modify-write cycle.
22. $t_{CAS}$ (min) = $t_{CWD}$ (min) + $t_{CWL}$ (min) + $t_T$ in read-modify-write cycle.

## Timing Waveform *23

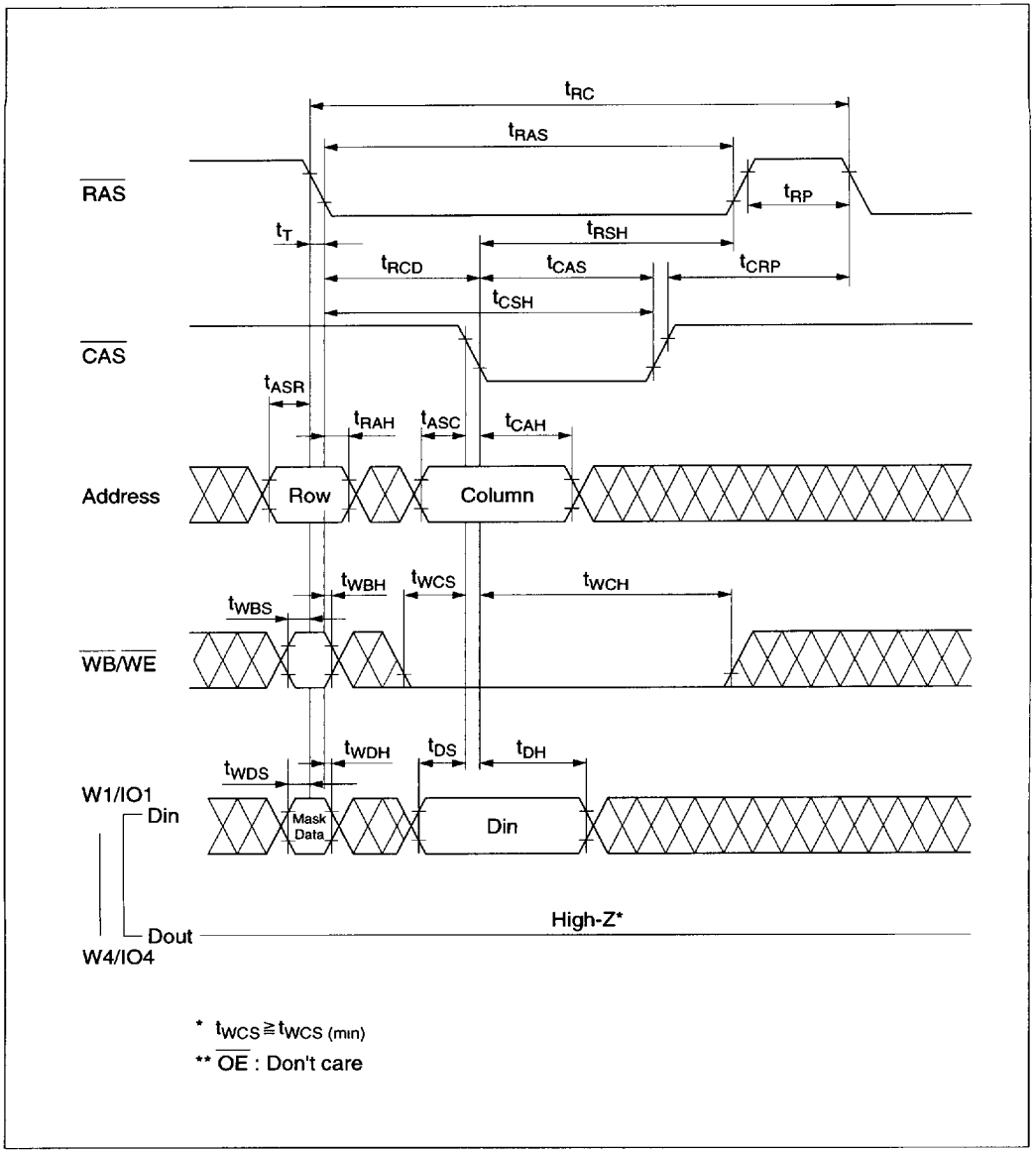
### Read Cycle




Notes: 23. : H or L (H : $V_{IH}(min) \leq V_{IN} \leq V_{IH}(max)$, L : $V_{IL}(min) \leq V_{IN} \leq V_{IL}(max)$)

: Invalid Dout

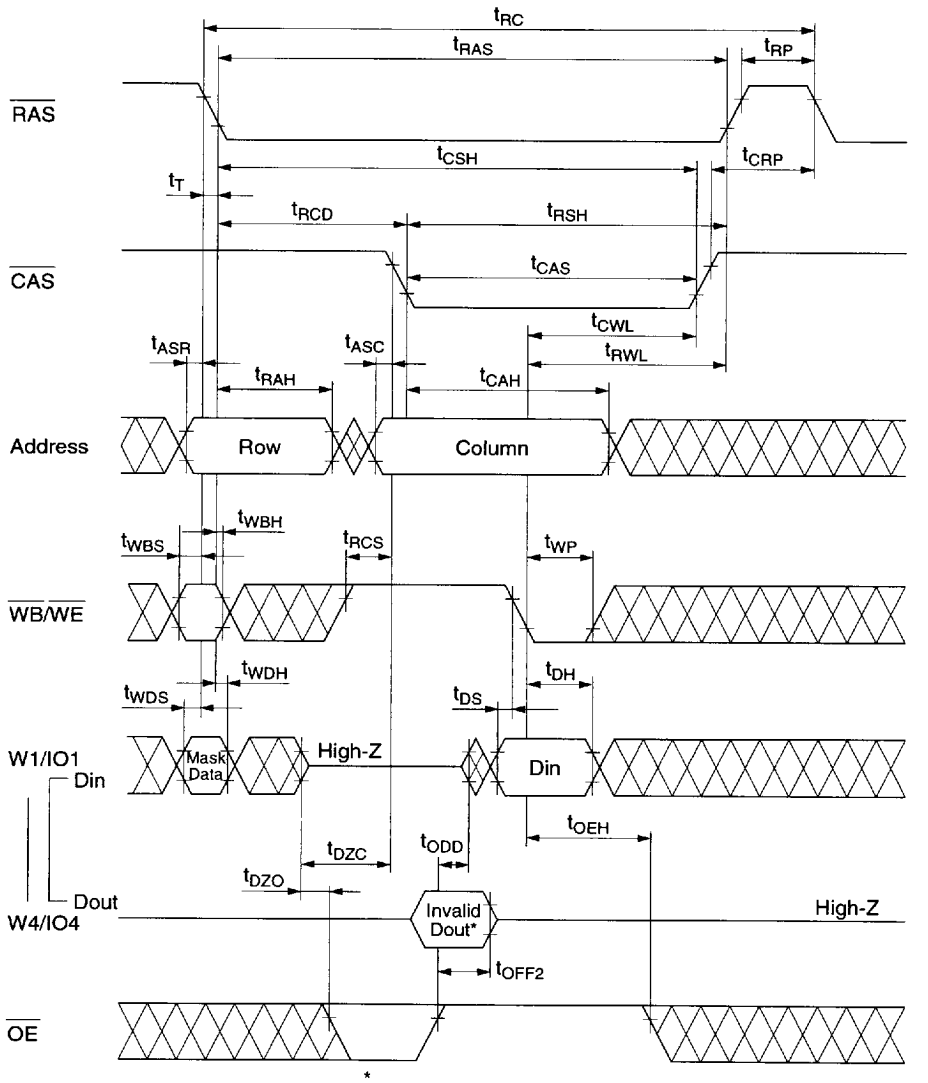
**Early Write Cycle**




* $t_{WCS} \geqq t_{WCS\ (min)}$

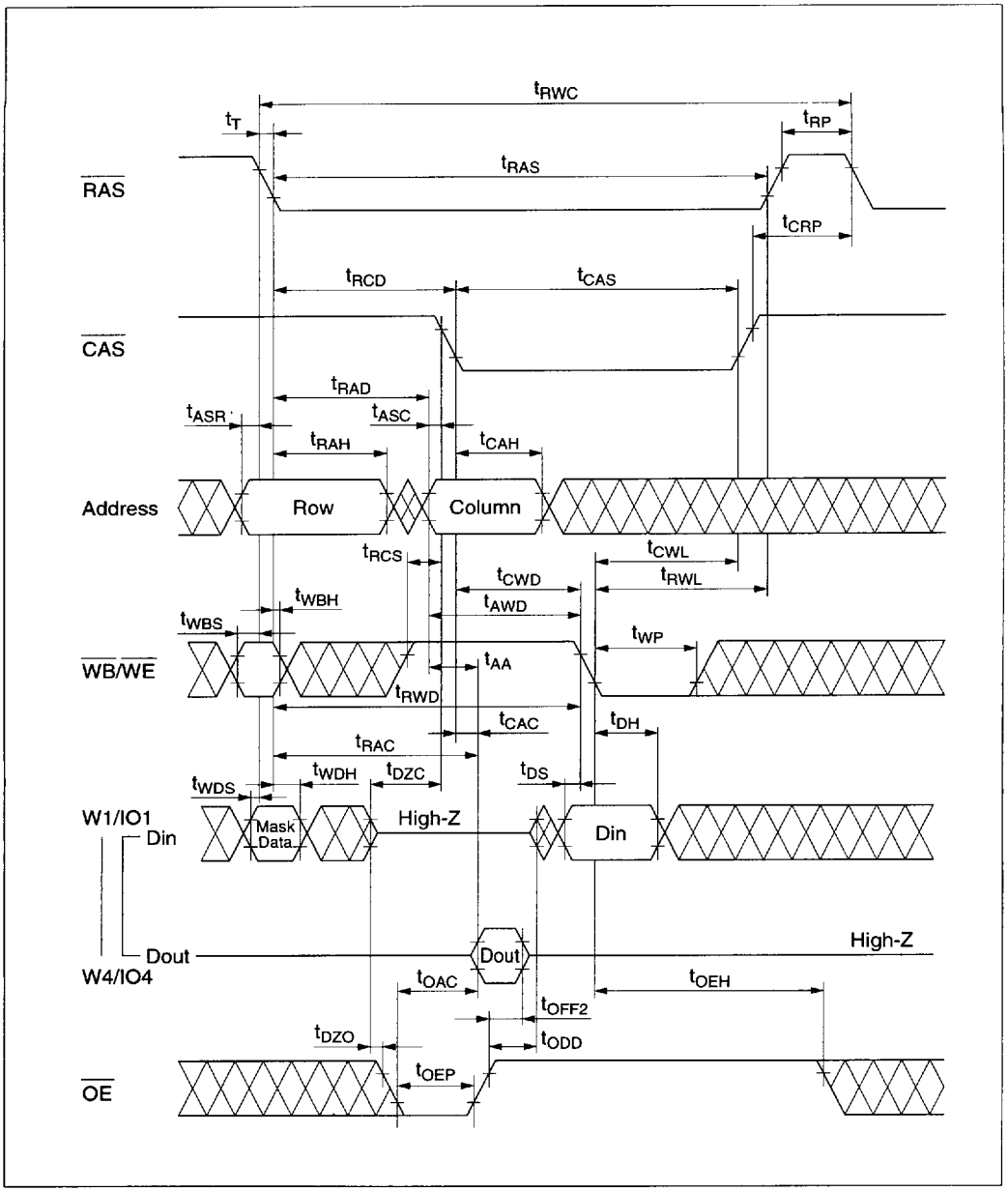
** $\overline{OE}$ : Don't care

**Delayed Write Cycle**

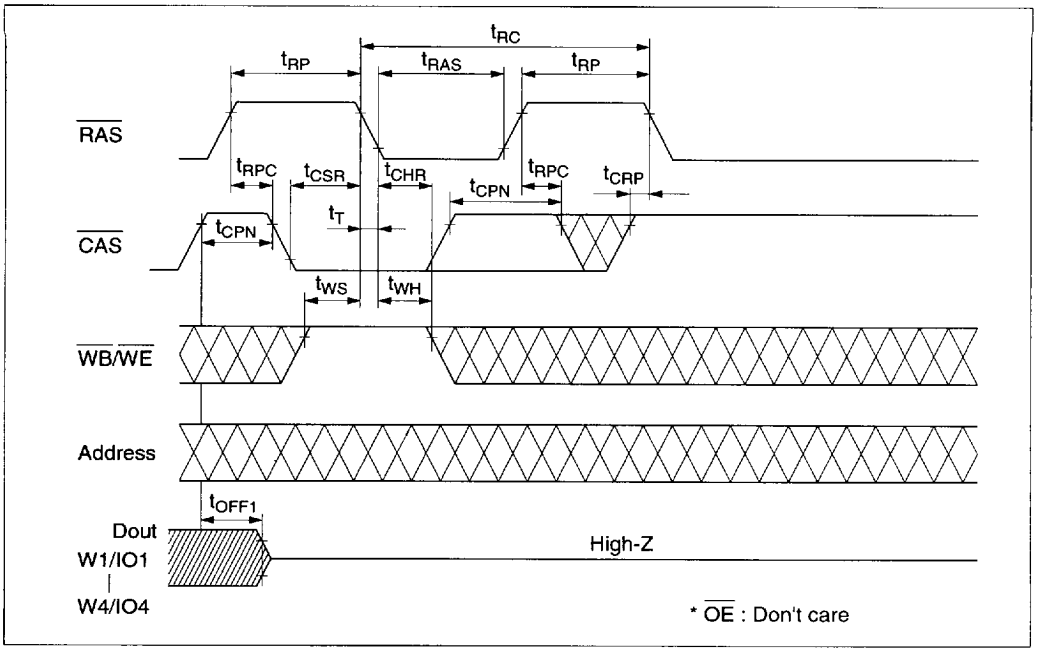



* Invalid Dout comes out, when $\overline{OE}$ is low level.

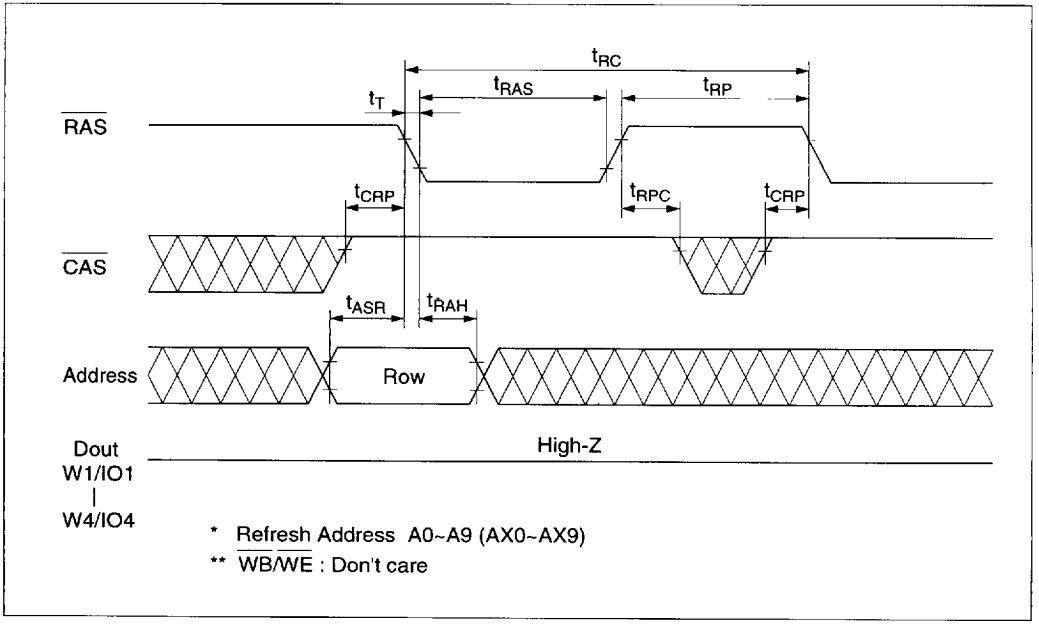
**Read-Modify-Write Cycle**



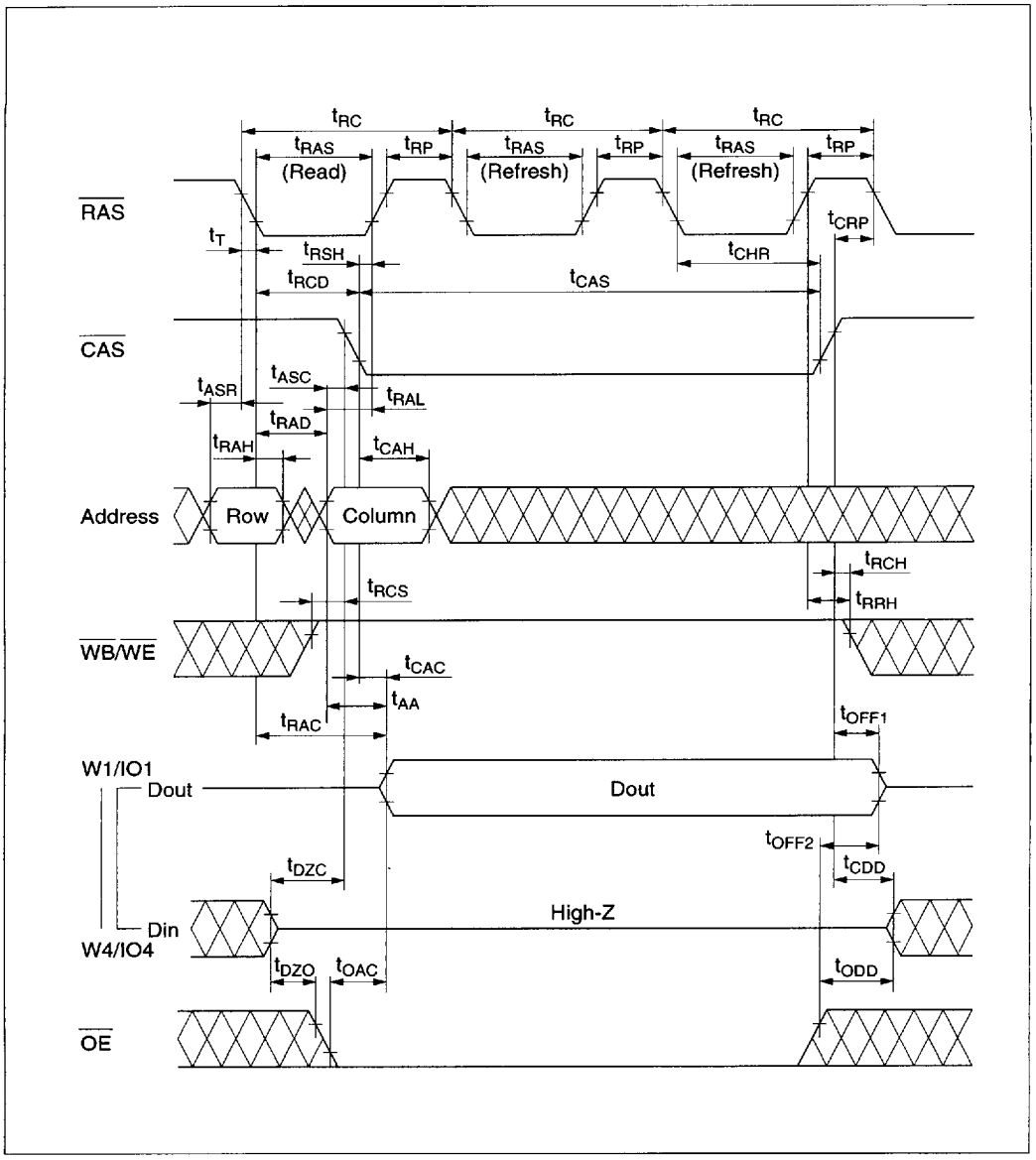
**$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle**



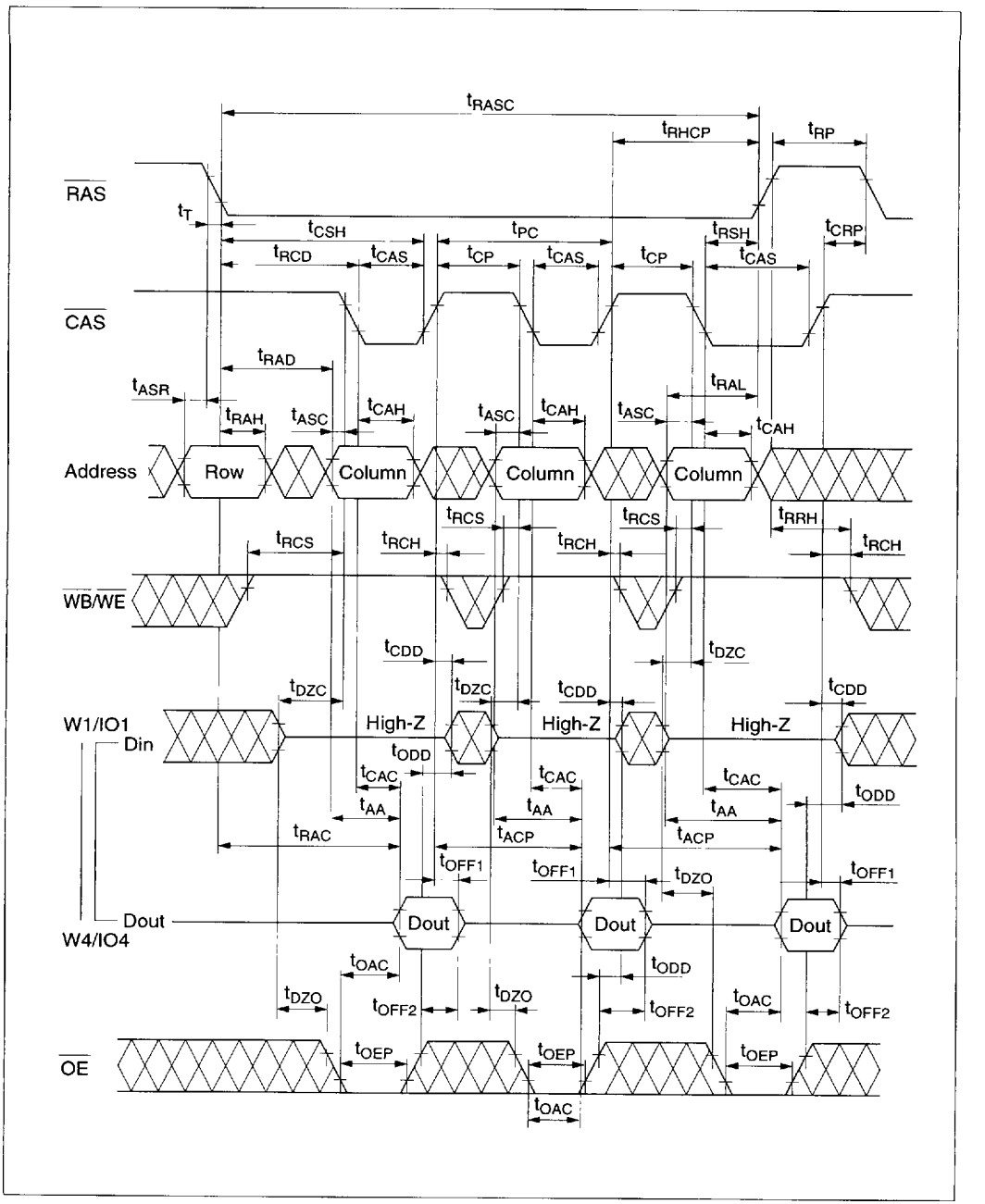

**$\overline{RAS}$-Only Refresh Cycle**



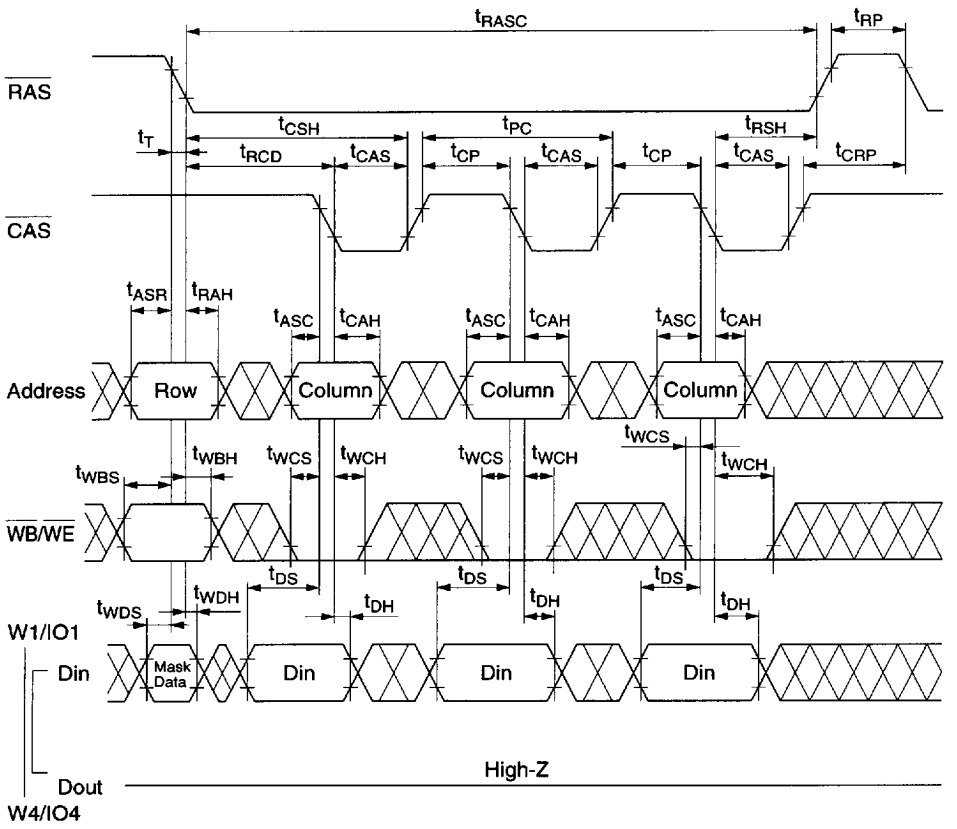
**Hidden Refresh Cucle**



**Fast Page Mode Read Cycle**

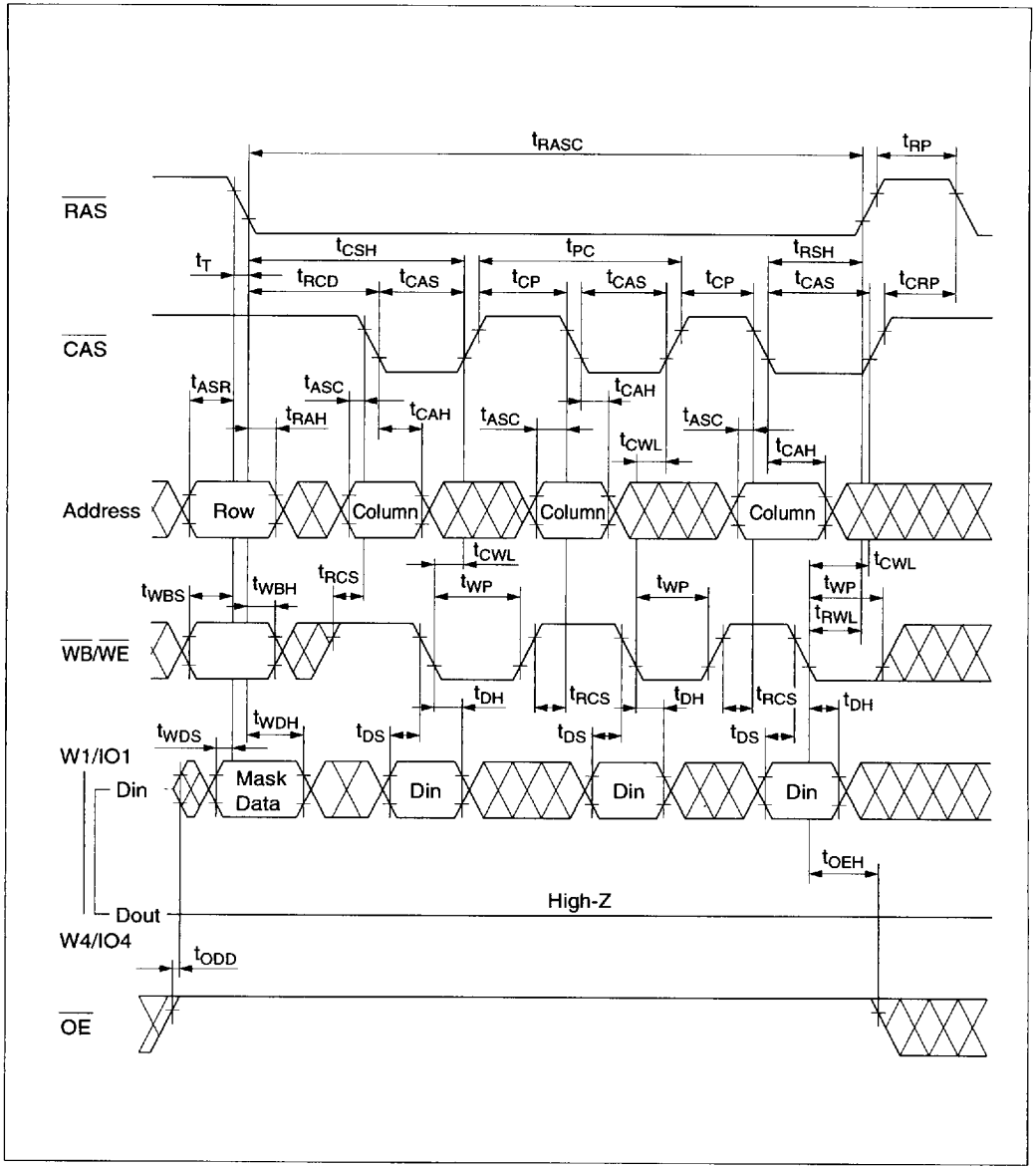


**Fast Page mode Early Write Cycle**

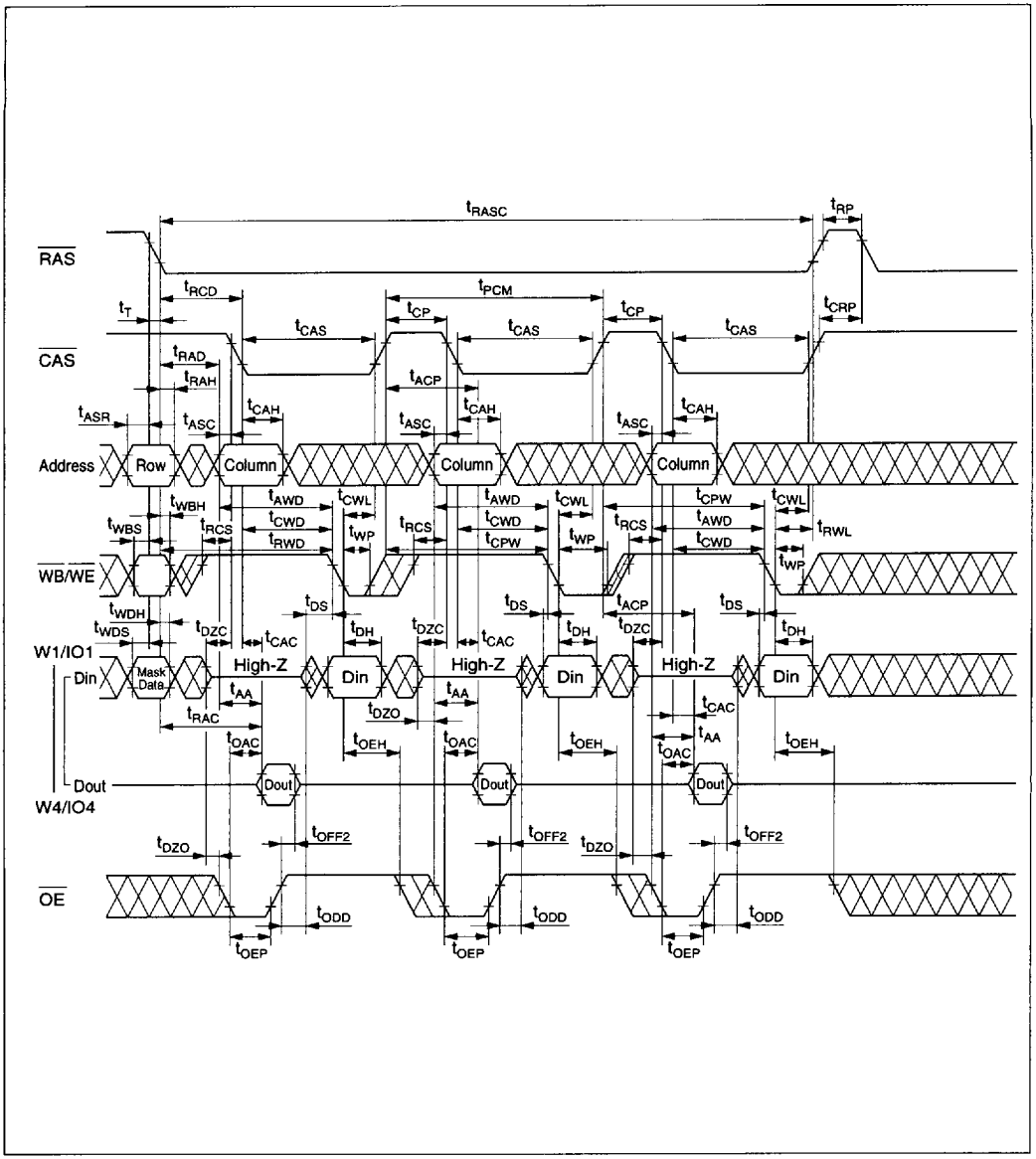



* $\overline{OE}$ : Don't care

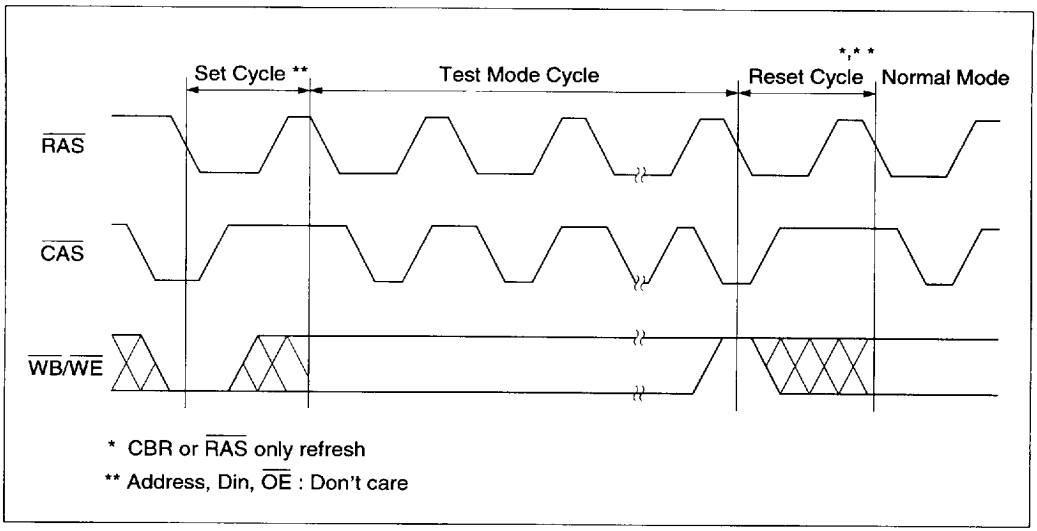
**Fast Page Delayed Write Cycle**



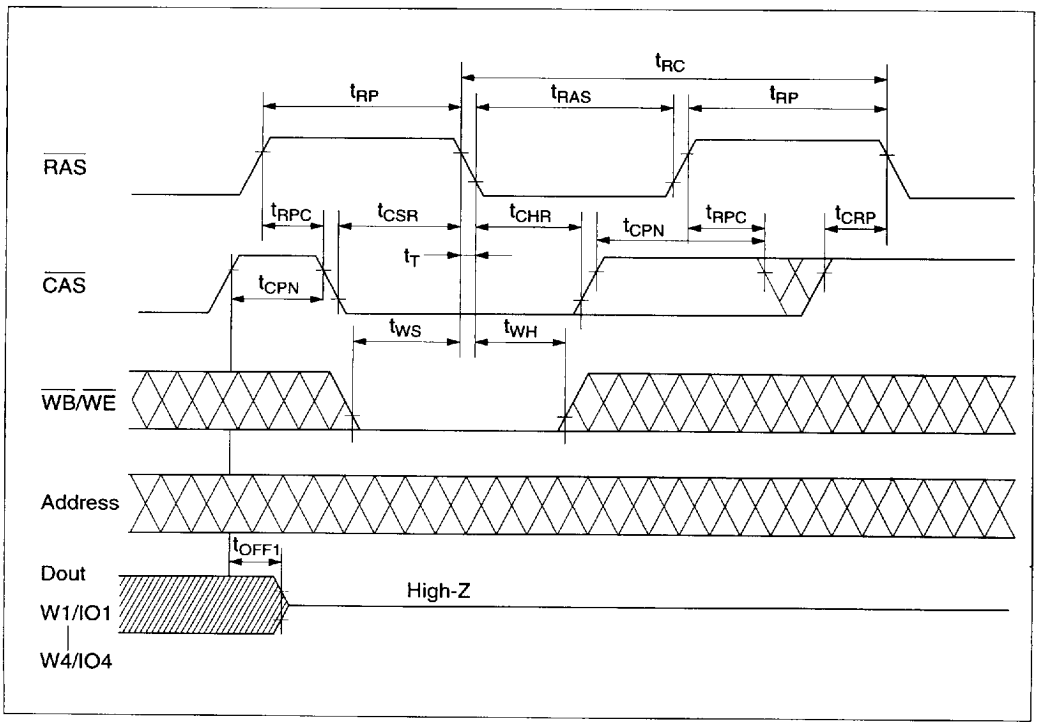
**Fast Page Mode Read-Modify-Write Cycle**



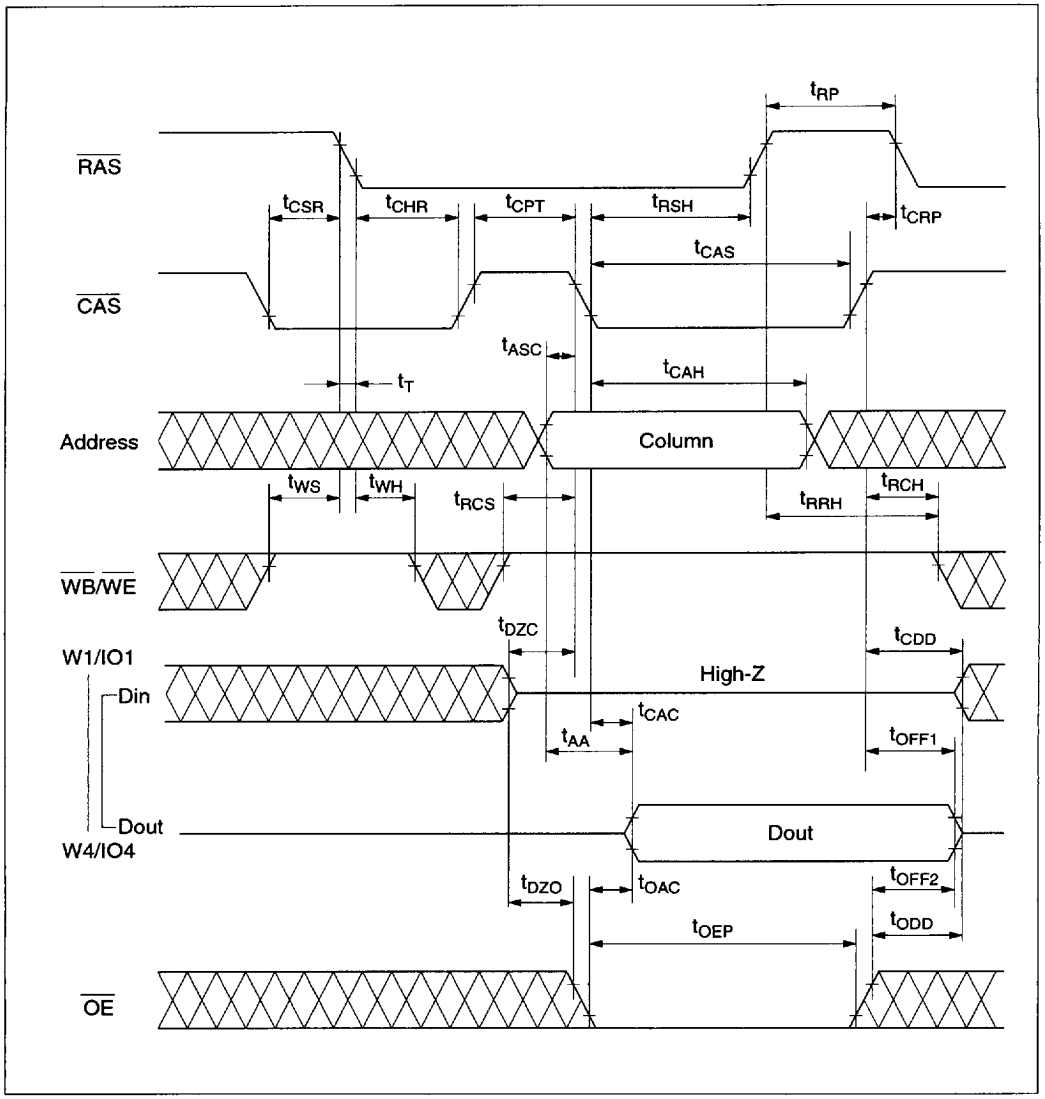
**Test Mode Cycle**




**Test Mode Set Cycle**



**$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Check Cycle (Read)**



**$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Counter Check Cycle (Write)**